What is Claimed is:

[c1] A two-terminal device comprising:

a nitride layer; and

a re-oxide layer on said nitride layer,

wherein said nitride layer and an interface between nitride layer and said re-oxide layer include electron traps.

[c2] The device in claim 1, wherein characteristics of said carrier traps control a voltage output of said device.

[c3] The device in claim 1, wherein a thickness of said nitride layer and said re-oxide layer control a voltage output of said device.

[c4] The device in claim 1, wherein said nitride layer and said re-oxide layer comprise one of a voltage regulator, voltage sensor, and memory device.

[c5] The device in claim 1, wherein said capacitor undergoes a trap filled limit voltage, such that a constant voltage is output for a plurality of currents.

[c6] The device in claim 5, wherein trap filled limit voltage events occur at different voltage levels, such that said device comprises a multi-value voltage regulator.

[c7] A capacitor voltage regulator device comprising:

a nitride layer; and

a re-oxide layer on said nitride layer,

wherein said nitride layer and an interface between nitride layer and said re-oxide layer include electron traps, and

wherein characteristics of said carrier traps control a voltage output of said structure.

[c8] The device in claim 7, wherein a thickness of said nitride layer and said re-oxide layer control a voltage output of said device.

[c9] The device in claim 7, wherein said capacitor undergoes a trap filled limit voltage, such that a constant voltage is output for a plurality of currents.

[c10] The device in claim 9, wherein trap filled limit voltage events occur at different

voltage levels, such that said device comprises a multi-value voltage regulator.

[c11] A method of manufacturing a capacitor structure, said method comprising:

growing a thermal nitride nucleation layer on a buried plate;

performing a low pressure chemical vapor deposition (LPCVD) of silicon nitride on said nucleation layer; and

re-oxidizing a top portion of said silicon nitride to form a re-oxide layer, such that said nitride layer and an interface between said silicon nitride layer and said re-oxide layer include electron traps.

[c12] The method in claim 1, wherein characteristics of said carrier traps control a voltage output of said device.

[c13] The method in claim 11, wherein a thickness of said nitride layer and said re-oxide layer modulate a voltage output of said device.

[c14] The method in claim 11, wherein said nitride layer and said re-oxide layer comprise one of a voltage regulator, voltage sensor, and memory device.

[c15] The method in claim 11, wherein said capacitor undergoes a trap filled limit voltage, such that a constant voltage is output for a plurality of currents.

[c16] The method in claim 15, wherein trap filled limit voltage events occur at different voltage levels, such that said capacitor device comprises a multi-value voltage regulator.